Modular thin-film memory system components...

by FABRI-TEK

Fabri-Tek has made available, in modular form the reliable FFM-202 Thin-film Memory System. Now, you can buy the thin-film memory modules you need to fit a particular design program.

For convenience of the design engineer, three basic levels of thin-film memory modules have been established by Fabri-Tek. Modification of these levels to fit special programs are, of course, available.

Level one

THIN-FILM PLANE OR STACK, ready to wire into your driver, selection, and sensing circuits.

Each plane contains 128 words of up to 39 bits each. You specify the stack needed for your 100 to 500-nsec cycle-time system, and Fabri-Tek will supply the module ready to wire or plug into your circuits.

This module offers an economical solution for small memory systems which are to share control circuitry.

Level two

THIN-FILM STACK PLUS BASIC ELECTRONICS, ready to plug into your input-output and control circuits.

This module consists of a thin-film stack plus all the drive, sense, and special circuits necessary to operate the stack.

This level is available from Fabri-Tek to those designers who wish to take advantage of the engineering, testing, and manufacturing experience that went into the production model FFM-202 system. The proven, reliable circuitry available with this module assures successful operation and integration of the thin-film memory into an overall system without extra design and development effort.

Level three

THIN-FILM MEMORY SYSTEM, complete with address register, timing and control circuits, power supply, indicators and self-test circuits.

This level of thin-film memory is a complete system, including timing and control circuits, data and address registers, and interface circuits. Indicators, power supply, and self-exerciser circuits are included.

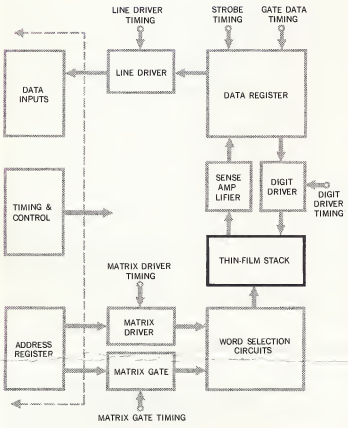
The Fabri-Tek FFM-202 series is a complete, production system. It is designed to fill the requirement for a 300-nanosecond full cycle with a 150-nanosecond access time.

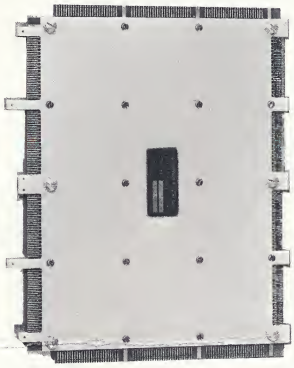
For the design engineer who desires a thin-film auxiliary storage register or high-speed buffer, complete and ready to run, this level is designed to fill his need.

Here's how you can buy and use

LEVEL 1

THIN-FILM STACK, ready to wire into your driver, selection, and sensing circuits.





10″ x 8″ x 5/16″ outline dimensions

FABRI-TEK Model FP12-12836 Memory Planes

Model FP12-12836 is a word organized, high speed destructive readout film memory plane. It is intended primarily for use in small memory systems with cycle times from 100 to 500 nanoseconds.

Each plane contains film core arrays sandwiched between two copper-insulator laminated overlays, on which the drive and sense lines are etched. Each plane contains 128 words of up to 39 bits each.

	Min.	Typ.	Max.	Units
Word Select Current	400	450	—	milliamperes
Digit Current	135	160	185*	milliamperes
Output**				
Amplitude	—	1.2	—	millivolts
Switching Time	—	20	—	nanoseconds
Drive line delay per bit	—	20	—	picoseconds

*The maximum digit current parameter is determined by a disturb test using greater than one million word select pulses of 20 ma amplitude combined with a reverse polarity digit current.

**The output is measured with a 450 ma word current and a 160 ma digit current. The word current rise time is 20 nanoseconds and the sense line is terminated in 50 ohms.

LEVEL 3

THIN-FILM MEMORY SYSTEM, complete with address register, timing and control circuits, power supply, indicators and self-test circuits.

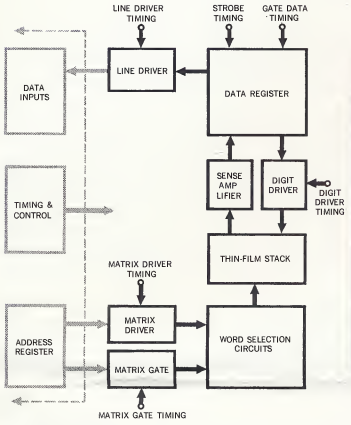
SERIES FFM-202 OPERATIONAL SPECIFICATIONS

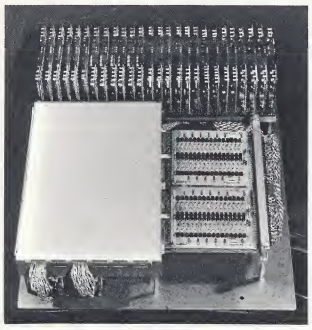
CYCLE TIME	300 nanoseconds full cycle. 200 nanoseconds read or write only.
ACCESS TIME	150 nanoseconds.
CAPACITY	Up to 512 words of 36 bits each.
OPERATING MODES	Read only, write only, read-restore, read-modify-write.
INPUT/OUTPUT LEVELS	Standard: 0 ±.5 volts and −4 ±.4 volts. Other levels can be provided as an optional feature.
CONTROL PANEL	Standard options: Address and data register indicators, voltage monitoring and fuses, self testing controls, error checking.
POWER REQUIRED	115 volts ac ± 10%, 48 to 63 cps. A typical 256-word, 36-bit system requires about 300 watts.

Fabri-Tek's thin-film modules

LEVEL 2

THIN-FILM STACK PLUS BASIC ELECTRONICS, ready to wire into your input-output and control circuits.





18" x 10" x 4" general package dimensions

Power Requirements For a Typical 256 x 18 System

+10 volts ± 2%	3.0 amps
−10 volts ± 2%	2.8 amps
−20 volts ± 2%	1.7 amps
− 4 volts ± 2%	4.1 amps

Logic Levels: 0 ±.5 v. and −4 ±.4 v.
(−4v. + 1, 0 v. = 0)

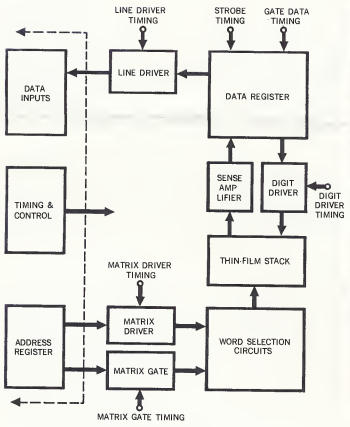
Data Inputs: 40 ma @ 0 volts for each bit line. This includes current supplied to 120-ohm termination resistor to −4 volts. The input data signals must be present and stable for the prescribed time interval of the write cycle.

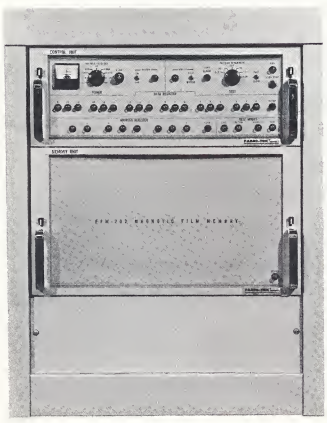
Address Inputs: Both true and complement are required. Each must supply 65 ma @ 0 volts including 120-ohm termination resistor to −4 volts. The address inputs must be present and stable for the prescribed time interval of both the read and write cycle.

Matrix Gate and Matrix Driver Timing: For each group of 256 words, two 80 ma @ 0 volt timing pulses are required. This includes the line termination resistor to −4 volts. This timing pulse is required for both the read and write cycle of operation.

Digit Driver, Gate Data and Strobe Timing: For each 6 bits of memory word length, a 70 ma @ 0 volts digit timing pulse; a 70 ma @ 0 volts gate data; and a 45 ma @ 0 volts strobe timing pulse is required. Termination resistors are included. The digit timing pulse is required for both the read and write cycle; the gate data timing is required for only the write cycle, and the strobe timing is required for only the read cycle of operation.

Line Driver: For each 9 bits in the memory word length, a 120 ma @ 0 volts line driver timing pulse is required. Termination resistors are included. The line driver timing is required only during the read cycle of operation.





19" relay rack mounting, 24" deep (includes cables), 17½" high

CONSTRUCTION

The system is packaged in two separate chassis. The upper drawer contains the power supply and the optional control and indicator circuits. The bottom drawer contains the memory stack and the basic memory circuits. The circuit boards, wiring, and memory stack are all readily accessible.

To avoid crosstalk problems, twisted pair or coaxial cable input and output lines are used. Line drivers capable of driving 150-ohm, twisted pair outputs are standard. Other packaging or input/output requirements can be provided as optional features.

OPERATION

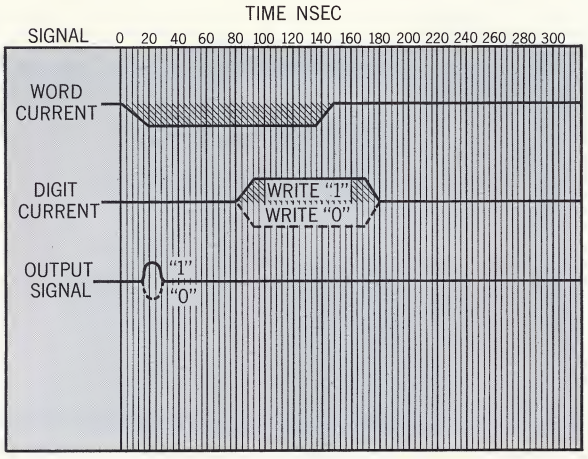
Since the memory system is word organized, it can tolerate wide variations in operating parameters. The nominal word select current is 450 ma. The nominal digit write current is 160 ma. These currents can typically vary ± 15% without loss of information.

The system can operate with either random or sequential address selection. In either case, the time duration of a normal read-restore cycle is 300 nanoseconds. The required input signals for this type of cycle are:

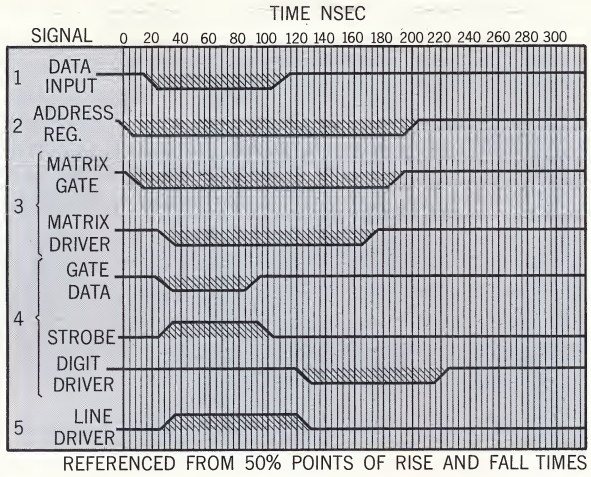
1. Initiate memory reference.
2. Mode select.
3. Address (random) or starting address (sequential).

OVER FOR MORE INFORMATION

Timing chart for Fabri-Tek's thin-film stack only. (Level 1)

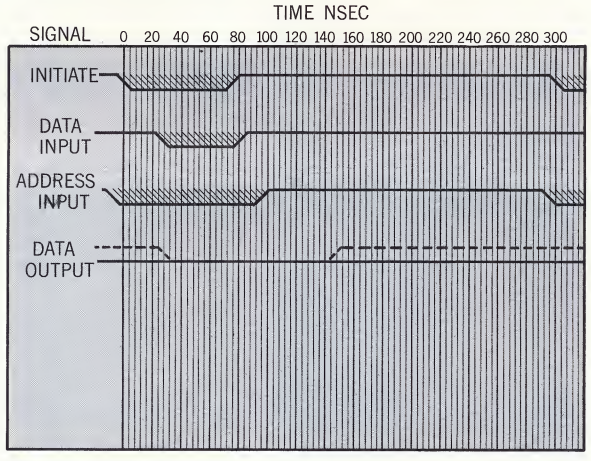


Timing chart for Fabri-Tek's thin-film stack plus basic electronics. (Level 2)



REFERENCED FROM 50% POINTS OF RISE AND FALL TIMES

Timing chart for Fabri-Tek's complete thin-film memory system. (Level 3)



For all of your requirements in non-rotating memories, look to Fabri-Tek!

FABRI-TEK INCORPORATED

FOSHAY TOWER • MINNEAPOLIS 2, MINNESOTA

Bulletin No. 6426

Printed in U.S.A.

PLEASE NOTE THE FOLLOWING CHANGES, WITH RESPECT TO PAGE 2 INFORMATION, AND PAGE 7 TIMING CHART:

ACCESS TIME SHOULD READ 350 TO 375 NSEC

HALF CYCLE TIME SHOULD READ 600 NSEC

The Series MFA1 coincident current core memory system

by FABRI-TEK

Here's a rugged Fabri-Tek memory system approaching "scratch pad" speed, yet it has a large memory capacity. It has a one microsecond cycle time and a 450-nanosecond access time. Word capacities range from 32 to 32,768 in any desired bit length.

The coincident current design takes advantage of the component economies inherent in this type of memory to provide large bit capacities with fewer selection components, resulting in improved reliability and simpler maintenance. Its fast cycle time serves to increase any basic overall system speed.

All-silicon semiconductor construction assures maximum reliability and longer life in the operating temperature range. The system is supplied in a standard RETMA relay rack chassis, 19 inches wide.

The Series MFA1 is ordinarily equipped with address and data register, power supply and self-test. The self-test feature, provides rapid, relatively easy trouble shooting and helps eliminate costly down time.

As in all Fabri-Tek coincident current systems, the Series MFA1 is designed to provide a versatile, "tailored" system while using proven concepts and components.

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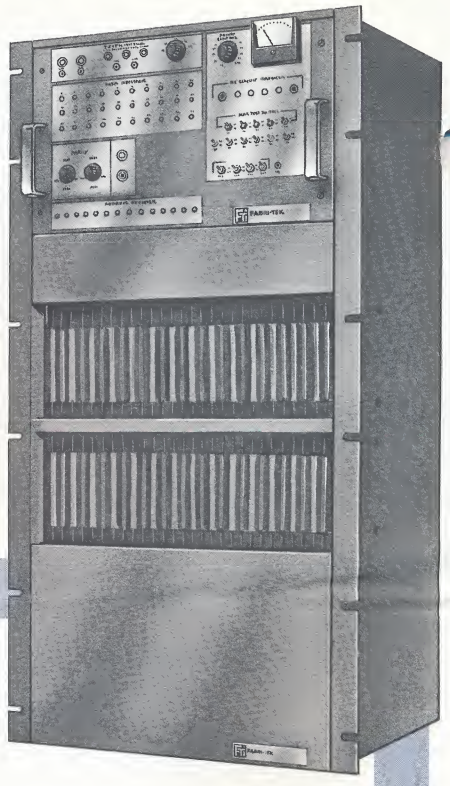
MFA1



SERIES MFA1 OPERATIONAL PARAMETERS

CYCLE TIME	Full cycle—1 usec Half cycle—450 nsec	
ACCESS TIME	450 nsec	
CAPACITY	32 to 32,768 words in any bit length	
ACCESS MODES	Random Sequential Random-sequential (All modes may be full- or half-cycle)	Sequential interlace Random-sequential interlace General purpose
COMMAND SIGNALS	See Timing Chart (Page 7)	
INPUT/OUTPUT LEVELS	Current or voltage interface levels are available Standard: 0 and +6 volts	
CONTROL PANEL	Address and data register indicators, voltage monitoring, power control switches, and self-testing controls	
SELF-CHECK PATTERNS	All ones. All zeros. Worst pattern. Worst pattern complement.	
POWER REQUIREMENTS	110 volts ac ± 10%, single phase, 50 to 400 cps A typical 4096 X 25 system requires less than 500 watts	

How to order a Series MFA system

Specify the exact MFA system you need by using the information in this brochure. The following part number key, made up of six elements, is used to identify the system characteristics you select. Each MFA system is supplied with quick disconnect type connectors. If desired, a connector wiring diagram and mating connectors will be supplied to you before delivery of the memory system. This will permit you to prewire the rack and have it ready when the MFA arrives.

1 — TYPE OF MEMORY AND CYCLE TIME

The first element of the part number contains a fixed code which describes the system. MFA represents this type memory system while the "1" stands for a cycle time of one microsecond.

2 — WORD CAPACITY

The second element represents word capacity. The MFA is available in word capacities of 32 to 32,768. These are coded as shown on page 4.

3 — BITS PER WORD

The third element represents the bit-per-word capacity. MFA systems are available in capacities that begin at 2 (code 02) and extend to meet customer requirements.

4 — CYCLE OPERATION

The fourth element describes the four cycle operations available. Specify full cycle as 0, half cycle as 1, both as 2, and split cycle as 3.

5 — OPERATIONAL MODES

This memory can be supplied in any of six operational modes. These are coded 1 through 5 and are described on page 4.

6 — OPTIONAL FEATURES

The MFA is ordinarily supplied with address and data registers, power supply and self-tester. However, the system can be ordered with any of these features deleted. The self-test feature can best be utilized in systems with a data register and address register. Ordering information is given on page 5.

MFA1	07	21	3	2	04

Typical part number describing a Series MFA coincident current memory system with a 1 microsecond cycle time, 4096-word capacity with 21 bits per word, full/half cycle operation, sequential access mode, and equipped with data and address register, power supply, and self-test.

Refer to Page 8 for data on optional features

Word Capacity

The MFA is available in capacities of 32 to 32,768 words.

For Word Capacity of:	Specify Type:
32	00
64	01
128	02
256	03
512	04
1024	05
2048	06
4096	07
8192	08
16384	09
32768	10

Bits Per Word

The MFA is available with bit capacities beginning at 2 bits per word (code 02). Specify the bit-per-word factor by simply including the number of bits as the third element in the part number. The bit code may be extended to more than two digits if necessary.

Cycle Operation

A. Full Cycle (Specify 0)

Two modes of operation are performed in a full cycle system; a read/restore mode and a clear/write mode. During a read/restore mode infomation is retrieved from memory storage from the specified address and made accessible at the data interface lines. Since the readout is destructive the restore portion of the cycle restores the retrieved data to the memory location. During a clear/write cycle the selected address location is cleared and the information which was loaded into the data register from the input data lines is stored in the same selected address location for later retrieval. Full cycle time is 1 microsecond or less depending on memory size.

B. Half Cycle (Specify 1)

A half cycle operation performs either a read only or a write only operation. During a read only operation data is retrieved from the memory storage at the specified address and made accessible to the data interface lines. All information previously stored at the selected address is lost during

Operational Modes

Specify number indicated as the fifth element in the part number.

A. Random (Specify 1)

In this type of memory system information may be stored and retrieved from any portion of the memory by random addressing. All memory cycles described above may be used in this mode of operation. Normal command signals required are the following:

1. Input Signals

a. Load sync pulse
b. Unload sync pulse
c. Data register input levels (1 or 2 lines per bit)
d. Address register input levels (1 or 2 lines per bit)

2. Output Signals

a. Data register output levels (2 lines per bit)

3. Optional Signals

a. Split cycle command
b. Address register clear
c. Data register clear
d. Memory clear

B. Sequential (Specify 2)

This system accepts information in a sequential manner during the load operation and inserts it into the memory in sequence starting at a specified address and proceeding to succeeding addresses as the address register is incremented. To unload, the address register is reset to the specified starting point and information previously stored is unloaded in sequence and in the order in which it was stored. Required command signals for this memory are:

1. Input Signals

a. Load sync pulse
b. Unload sync pulse
c. Data register input levels (1 or 2 lines per bit)
d. Address register clear

2. Output Signals

a. Data register output levels (2 lines per bit)

3. Optional Signals

a. Address markets (Specifying start and stop locations)

a read only operation, and all bits at the address are set to 0. Cycle time is 550 nanoseconds. During a write only cycle data presented to the memory from the data input lines restored in the memory storage at the specified address, prior to a write only operation. The memory storage at that location must be cleared to 0 to prevent alteration of data. Write only cycle time is 600 nanoseconds.

C. Full- and Half-Cycle (Specify 2)

A combination full- and half-cycle operation is also available. An additional interface line may be required for the memory to switch to one type of operation to the other.

D. Split Cycle (Specify 3)

The split cycle operation, more commonly referred to as a read/modify/write or a read/alter/rewrite cycle, permits modification of data after the data is retrieved from the specified memory location and prior to being restored to that same location during the restore portion of the cycle. In general a split cycle will be longer than the normal one microsecond and the total cycle time will be determined by the duration of the modified time of the cycle. An additional interface line is required for this type of cycle over the two command lines required for a full cycle operation.

C. Random and Sequential (Specify 3)

This system provides for operation in both of the modes described above.

D. Sequential Interlace (Specify 4)

This is very similar to sequential access (type 2) except that information may be loaded and partially unloaded at will. A second address register makes this possible. The last storage location for load or unload information is retained in each respective address register. As in the non-interlaced system, the information is loaded sequentially and unloaded sequentially in the order in which it was stored. Input/output commands are the same as those required for the sequential, non-interlaced system.

E. General Purpose (Specify 5)

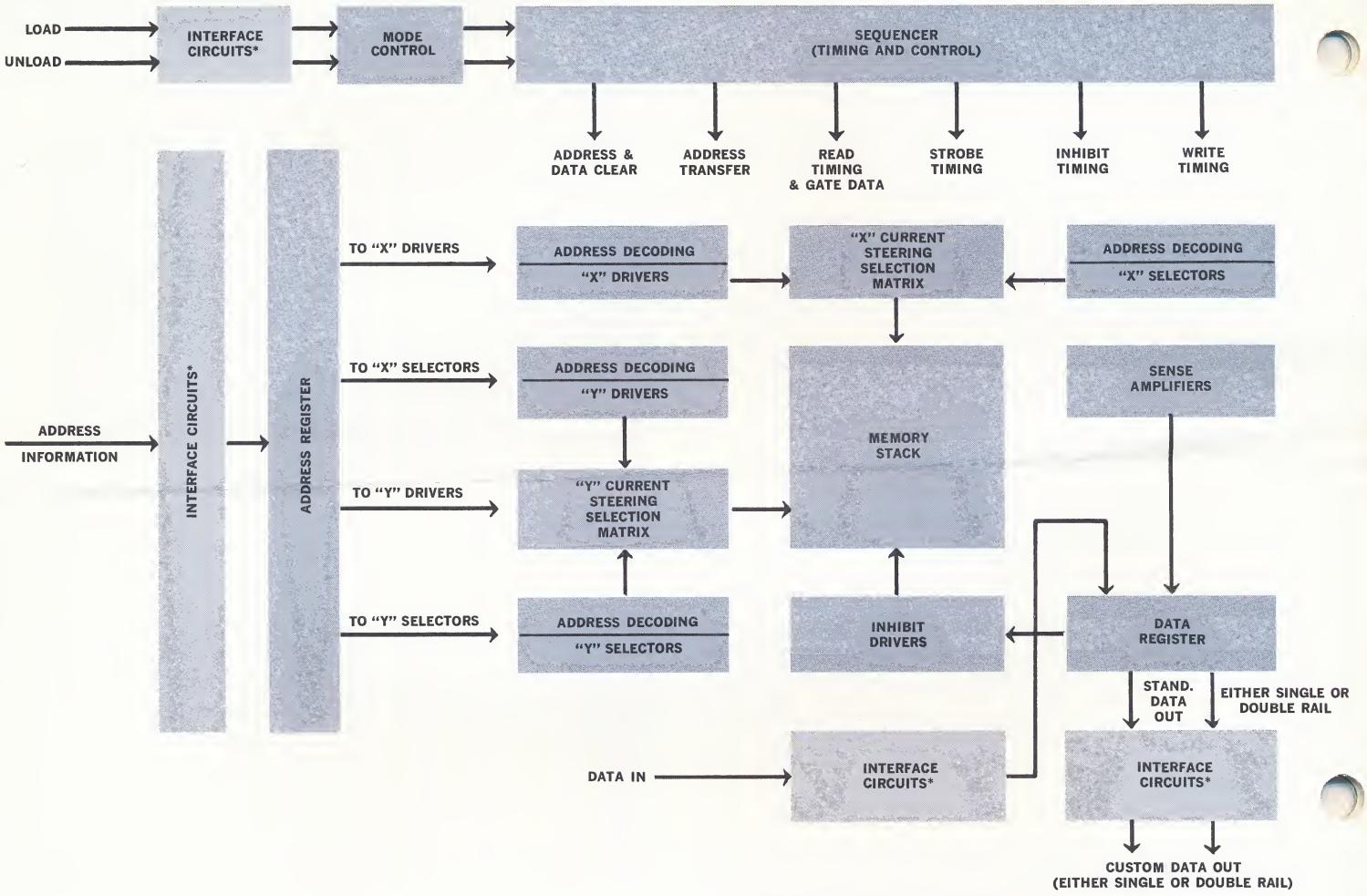
For greatest versatility, Fabri-Tek Incorporated Series MF memory systems are available in general purpose configurations which are capable of any of the above modes of access. Interface commands required are those described in the foregoing descriptions. There may be any combination of any of the three modes of operation (random, sequential, or interlaced) with any of the cycles described. This provides the user with a versatility to adapt the memory system to his particular specifications.

Address Register, Data Register, Power Supply and Self-Test

The Series MFA is ordinarily equipped with address register, data register, power supply, and self-test, since most users require these features. Your Series MFA can, however, be furnished with any combination of these. The sixth element of the part number describes such combinations. For instance, if you require a system incorporating all four of these, then specify 04 as the sixth element in your part number. If you want only the data register, specify type 05. Other combinations are: shown below.

1. For Series MFA equipped with: / 2. Specify Type:	ADDRESS REGISTER	DATA REGISTER	POWER SUPPLY	SELF-TEST
00				
01	■			
02	■	■		
03	■	■	■	
04	■	■	■	■
05		■		
06		■	■	
07			■	
08	■	■		■
09	■		■	

Series MFA system



*CUSTOM INTERFACE CIRCUITS ARE AVAILABLE AS LEVEL SHIFTERS OR TO MEET THE REQUIREMENTS OF THE ASSOCIATED EQUIPMENT.

GENERAL SPECIFICATIONS

Environmental:

Operating Temperature (Standard)—
+10°C to + 40°C

(With optional heated stack)—
—0°C to +55°C

Relative humidity—90 percent without compensation

Vibration—10 G's standard commercial

Shock—15 G's standard commercial

Physical Specifications:

Depth—20 inches maximum

Height—varies with memory capacity

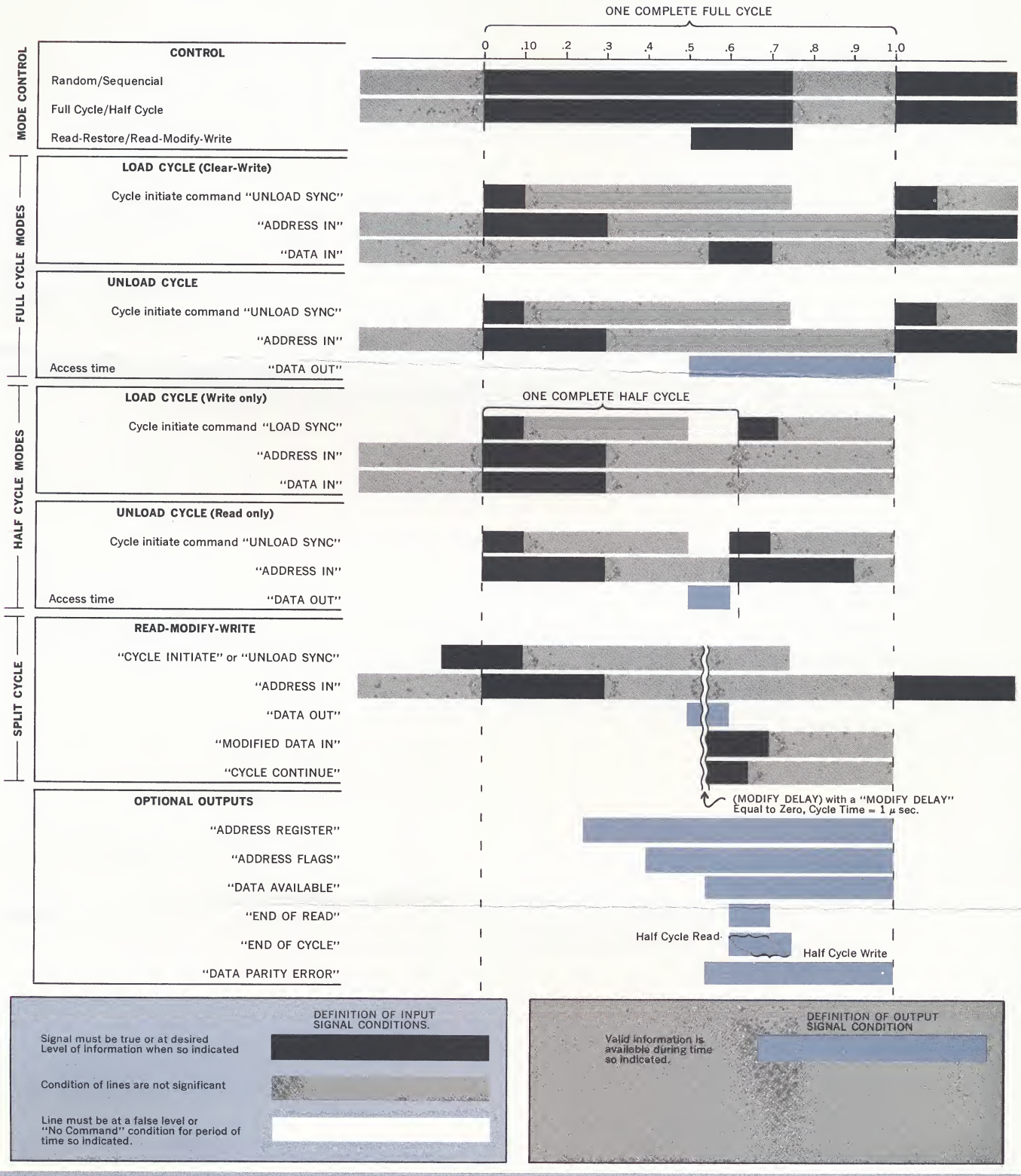
Width—19 inches, fits standard RETMA relay rack

Finish—Gray, baked vinyl enamel (unless otherwise specified)

Circuitry—Silicon semiconductor printed circuit modules, wire wrap interconnections between chassis locations. Test points located at front edge of all modules.

Interface—Interface lines may be quickly disconnected by means of connectors. All signals to and from the memory are transmitted by terminated, twisted pair lines or coaxial cables.

MFA1 MEMORY SYSTEM Timing Chart INTERFACE SIGNAL



NOTE

Timing shown indicates signals of minimum duration for a standard system. Systems are available with other variations which will meet optimum requirements of the associated data processing equipment.

Optional Features

To Specify . . . After selecting the MFA system to satisfy your requirements, choose any or all options from the following list. To specify, simply call out the basic Series MFA and state the optional features by letter. For example:

MFA1 07 21 3 2 04 with options A,C,D, (odd) and G

A. **Memory Clear**—Single command clearing of all cores of the memory stack to zero.

B. **Flag Signal**—Signals to the interface are available which indicate the addressing of specified addresses. Flags may be gated to indicate the given address during load and/or unload as specified. Any number of flag signals may be specified.

C. **Parity Check**—Odd or even parity check is available for error checking of the data and/or address.

D. **Parity Generate**—One bit of each word may be designated as a parity bit and an odd or even parity generated and stored in that bit. This bit is later used with the parity check feature for parity checking of the data stored in the memory.

E. **Marginal Voltage Check**—1. Separate controls may be provided for each DC logic voltage to allow simultaneous switching of any or all voltages to ± 5 percent of nominal values.

2. Individual margin checking of all DC logic voltages to ± 10 percent of nominal values is available, using a single preset front panel control.

F. **Data Saver**—The Fabri-Tek "Data Saver" data retention circuit provides 100 percent protection of data contained in the system during AC power failure or severe line transients. Data contained in the data registers of the systems will be returned to the memory, prior to shut down during a power failure.

In addition to the automatic protection of the "Data Saver", signals indicating "Power is Failing" and "Power has Failed" may be specified. Such signals brought to the interface will provide for immediate recognition of a power failure.

G. **Wide Temperature Operation**—Compensation for temperature variations is available to allow for operation of the system in temperatures between 0°C to +55°C.

H. **Manual Load**—Manual insertion of random information into any address from the systems control panel is possible by use of the optional "Manual Load" feature. Push button indicators provide for manual selection of any address and setting of any combination of data into the data register. A single operation of the "Stop/Step" switch will load the data into the selected address.

Manual selection of any given address as indicated above may also be used for manual sampling of any information stored in the memory. With the system in "Unload," the data stored in a selected word can be read-out and displayed on the control panel.

For all of your requirements in non-rotating memories, look to Fabri-Tek!

FABRI-TEK® INCORPORATED

FOSHAY TOWER • MINNEAPOLIS, MINNESOTA 55402 • PHONE 612-336-1646

Printed in U.S.A.

FABRI-TEK INCORPORATED

REPLY CARD

☐ MY NAME AND ADDRESS IS CORRECT

☐ CORRECT TO

NAME _____

DEPT. _____ PHONE NO. _____

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP CODE _____

ABOUT THIS REQUEST

- ☐ We received the data you sent
- ☐ Information is adequate
- ☐ Add my name to mailing list
- ☐ We need additional information – call me
- ☐ This is for an immediate requirement
- ☐ Need price and delivery information
- ☐ Need technical assistance
- ☐ This is for a future project due Date: _____
- ☐ We need some application assistance
- ☐ This is for literature files only

MR. T. NELSON, CONSULTANT
BOX 1546
POUGHKEEPSIE, NEW YORK

OUR REFERENCE A0250

DATED May 26, 1959

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AMERY, WIS. 54001

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AMERY, WISCONSIN 54001

FABRI-TEK INCORPORATED • FOSHAY TOWER • MINNEAPOLIS, MINNESOTA 55402 • TELEPHONE 336-1646

MR. T. NELSON, CONSULTANT
BOX 1546
POUGHKEEPSIE, NEW YORK

OUR REFERENCE: A0260

DATED: MAY 26, 1965

REFERENCE: 1,500,000 BIT

DEAR SIR:

Attached is the technical information you requested.

May we at be of further service to you:

- Technical assistance from one of our applications engineers on your particular application?
- Price and delivery information?

IN ORDER THAT WE DO NOT CONTACT YOU UNNECESSARILY, MAY WE SUGGEST YOUR RETURNING THE ENCLOSED REPLY CARD.

Very truly yours,

Robert F. Stahl Jr.

Robert F. Stahl, Jr.
General Sales Manager

YOUR NEAREST FABRI-TEK SALES OFFICE:

WILD & ASSOCIATES
1519 NORTHERN BLVD.
ROSLYN, LONG ISLAND NEW YORK

PLEASE REPLY TO: AMERY, WISCONSIN 54001 • Telephone 715-268-7155 • TWX 715-292-0900

The Series MLA5 integrated-circuit core memory system

by FABRI-TEK

The Fabri-Tek Series MLA5 memory system uses integrated circuits in memory logic, decoding, timing and interface to take maximum advantage of their low cost, low power consumption, and space-saving capabilities.

The Series MLA5 is now available in selected capacities as a plug-in, relay-rack module. Intended for commercial and industrial use where cycle times of 5 microseconds or longer are acceptable, the Series MLA5 offers smaller size, greater reliability, lower power dissipation, and lower cost than previous coincident-current core memory systems.

Series MLA5 systems are all packaged in a standard-sized, relay-rack type chassis, 5-7/32″ high by 19″ wide.

Capacities available are: 128, 512, and 2048 words with 2 to 26 bits per word, in increments of 2 bits. A choice of two input and two output interface circuits and optional address register is offered. Separate power supply and portable exercisers are optional equipment.

The Fabri-Tek Series MLA5 memory system has been engineered to provide maximum reliability and economy for a particular set of standard requirements. It does present the systems design engineer with a standard, off-the-shelf, memory system that is unsurpassed by any memory having comparable design parameters.

How to order a Series MLA5 system

You can specify the exact MLA5 system you need by using the information in this brochure. The following part number key is used to identify the particular system you select. Each MLA5 system comes equipped with mating connectors for wiring into your relay rack equipment. If you desire, a connector wiring diagram for your specific MLA5 system will be forwarded before delivery of the equipment to enable prewiring of your rack, ready to plug in the MLA5 when it arrives.

1 The first four numbers of the part number are fixed for the memory system series covered in this brochure. The "ML" stands for this general series of systems. "A" stands for the standard relay-rack physical packaging. "5" means a 5-microsecond cycle time system.

2 Word capacities are available in 128, 512, or 2048 words only. The code number 02 stands for 128 words, 04 stands for 512 words, and 06 stands for 2048 words.

3 The next number in the part number represents bits per word. The Series MLA5 is available in bit sizes of 2 to 26 bits in increments of 2 bits, i.e. 2, 4, 6, 8, 10, etc. Code numbers start with 02 for two bits to 08 for 8 bits. From 10 to 26 bits the actual number of bits is the code number.

4 Input interface circuits are coded by the next number. The two types of circuits are described on pages 6 and 7 of this brochure. Code number for the "standard" input interface circuit is "0". Code Number for the "custom" input interface circuit is "1".

5 The next part number code stands for output interface circuit. See pages 6 and 7 for a description of the two output interface circuits available. The code "0" represents the "standard" output interface circuit. The "custom" output interface circuit is specified by a "1".

6 The Series MLA5 can be obtained with or without an address register. The code number "0" calls for *no* address register. A figure "1" specifies an address register.

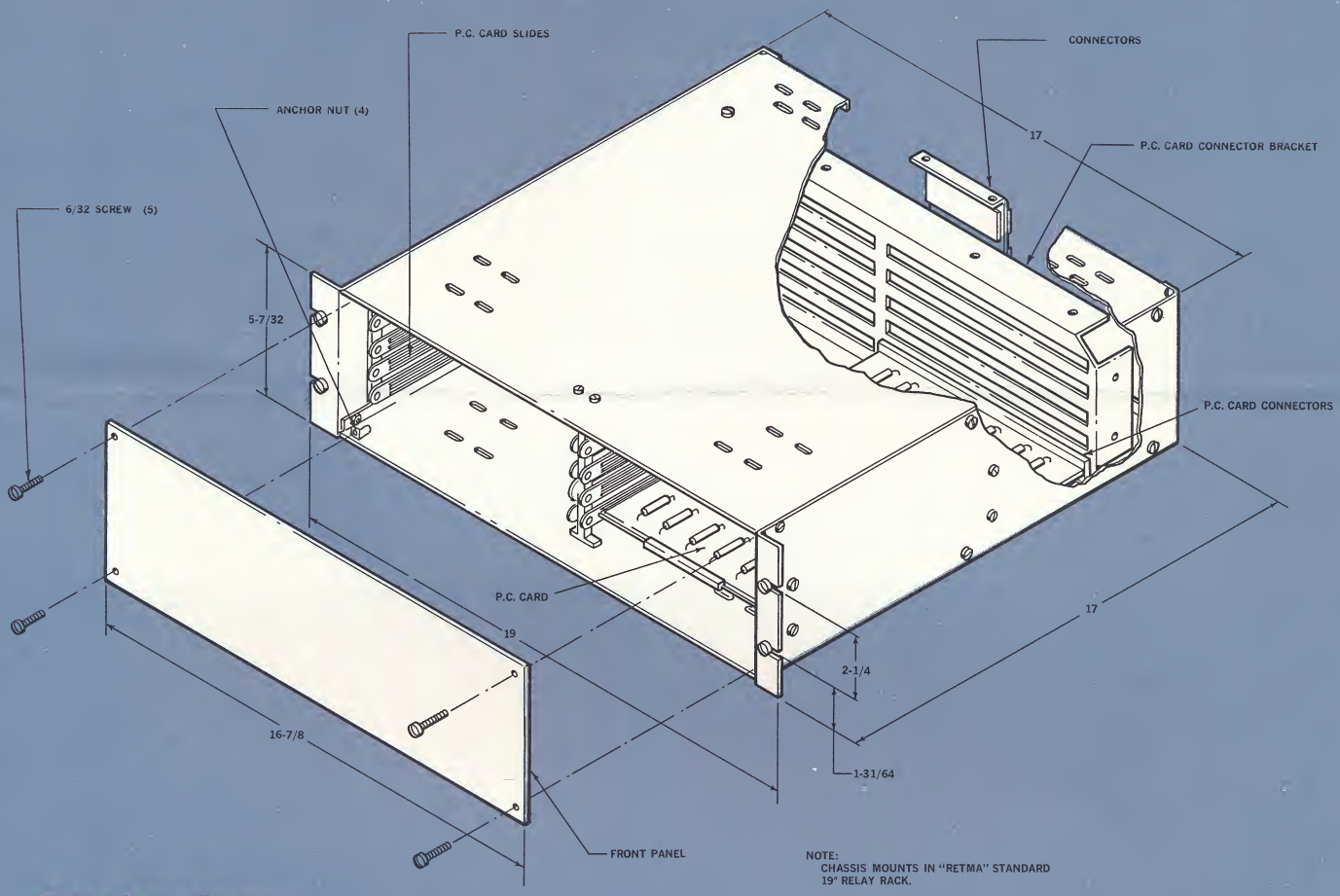
MLA5 02 02 0 0 0

Separate power supply and portable exerciser may be ordered separately.

A typical part number

MLA5	02	02	0	0	0
Series ML in standard relay-rack mounting 5-usec cycle time	128 words	2 bits per word	"standard" input interface circuit	"standard" output interface circuit	no address register

Physical configuration, speed and capacity



Packaging

The figure above illustrates the standard relay-rack package for all Series MLA5 systems. Mating connectors are supplied with each system.

Speed

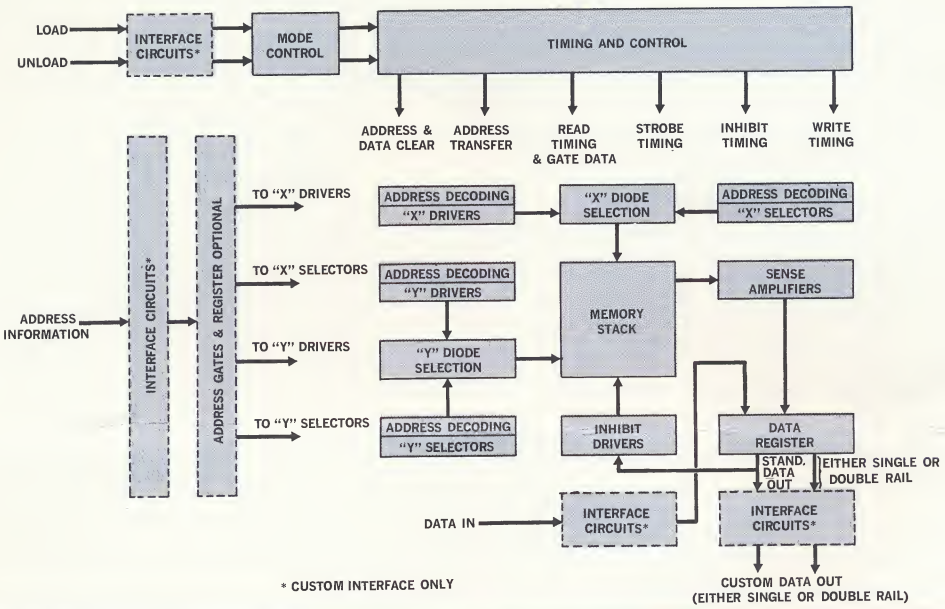
All MLA5 systems have a 5-microsecond full cycle time. Full cycle systems utilize two modes of operation—clear-write and read-restore. The clear-write mode is used when the memory is to be loaded. The "clear" part of the mode prepares the cores at a selected address to accept the information to be stored. The "write" part of the mode loads information into the cores. The read-restore mode is used in retrieving the information stored in the memory. Since the "read" operation necessitates destruction of the stored information, it is necessary to "restore" the read-out information immediately so that it can be read-out again at a future time. The clear-write and read restore operations are initiated by a load or unload initiate pulse, respectively. It requires 5 microseconds to perform one complete mode, clear-write or read-restore.

Capacity

The Series MLA5 system is available in these capacities only: 128, 512, 2048 words of from 2 to 26 bits in increments of 2 bits.

If your word and bit requirements are not exactly these, select a system which has the next higher capacity than you need. The systems are designed to be used this way and it is more economical than asking for a "special".

SERIES MLA5 SYSTEM



A block diagram of the Series MLA5 system is shown above. The timing and control section produces the control pulses and pulse levels necessary to operate the system. These signals are charted in relation to each other on the opposite page.

ADDRESS DECODING

Address information is decoded in the "X" and "Y" driver and selector circuits. Decoding is performed by multiple "and" gates. The larger drive current needed to switch cores is produced by a high-current transistor in the final stage of the current driver.

MEMORY OPERATION

The activation of a given set of "X" and "Y" drivers and "X" and "Y" selectors produces "half-currents" coincident at a specific core location in each plane of the memory stack. "Half-currents" are not sufficient to switch cores unless two "half-currents" become coincident at a given core. Coincidence is a function of the address information.

"X" and "Y" diode selection matrices are used to reduce the number of drivers and selectors required to drive a core memory plane. Diodes are used in the selection matrix to block drive current from passing through unselected drive lines.

The memory cycle consists of two parts—a clear or read portion and a write or restore portion. These portions are combined to make a clear-write mode or a read-restore mode, depending upon which initiate input line is pulsed. The load initiate pulse triggers a clear-write cycle and an unload pulse triggers a read-restore cycle.

During the clear or read portion of the memory cycle, all selected cores (determined by the address information) are switched to the "zero" state. This serves two purposes. First it permits the sensing of all cores which were in the "one" state (reading) and second, clears all the cores to the "zero" state in preparation for writing or restoring, as the case may be, during the last portion of the cycle. During this first part of the memory cycle, either the output of the sense amplifiers (in case "ones" were read and are to be restored) or the input of the data input lines (in case the memory is to be cleared for writing) are transferred to the data register.

During the write or restore portion of the memory cycle, the "X" and "Y" currents are reversed. If no other currents are present, this will cause the selected cores (determined by the address information) to be switched to the "one" state. However, in those planes where an inhibit current is present, the effect will be to cancel one of the "half currents," leaving those cores in the "zero" state.

The inhibit driver acts under the control of the data register. If a "one" bit has not been placed in the data register, either by reading the memory or by input lines, an inhibit current is generated which prevents cores in the associated bit plane from being switched to the "one" state.

Thus, a complete memory cycle can be either the clear-write mode or the read-restore mode, depending upon the combination of the clear or read portion and the write or restore portion of the cycle.

CIRCUITRY

Integrated circuits are used in the timing and control sections, data register, first stage of the inhibit driver, final stage of the sense amplifier, and in the address decoder circuits. The first stages of the sense amplifiers are discrete-component, differential amplifiers with negative feedback for gain stabilization.

ADDRESS REGISTER

If it is not practical to provide address information to the Series MLA5 memory for the times illustrated in the timing chart opposite, an internal address register should be specified when ordering an MLA5 system. If an external address register is used, only the "true" side of the address need be brought into the memory system. A gate will transfer address information to the internal register and the external register or counter can be changed during the remainder of the memory cycle. If no internal address register is specified, both the "true" and "complement" of the address lines must be brought into the memory system.

SIGNAL LEVELS

In the Series MLA5 system, a true signal ("1") is a low-voltage level and a false signal ("0") is at a high-voltage level. However, the signal-level definition "1's" and "0's" in the MLA5 system does not have to coincide with the signal-level definitions for "1's" and "0's" in the remainder of a data-processing system. The MLA5 memory system will return to external equipment the same voltage levels introduced to the system for storage. So, if a ground potential were presented to the memory system for storage, the "true" side of the data register would be at ground potential upon retrieval of the stored information. Conversely, if a high-voltage level were to be stored, the true side of the data register would be at a high-voltage level upon retrieval.

The internal logic level in the Series MLA5 memory system is zero and plus 3.6 volts. Supply voltages for the memory are plus 3.6, plus 12 and minus 12 volts d.c. The current requirements for the various memory sizes are shown in the table opposite. If a separate power supply is ordered from Fabri-Tek, these power requirements are satisfied by the separate unit.

Description

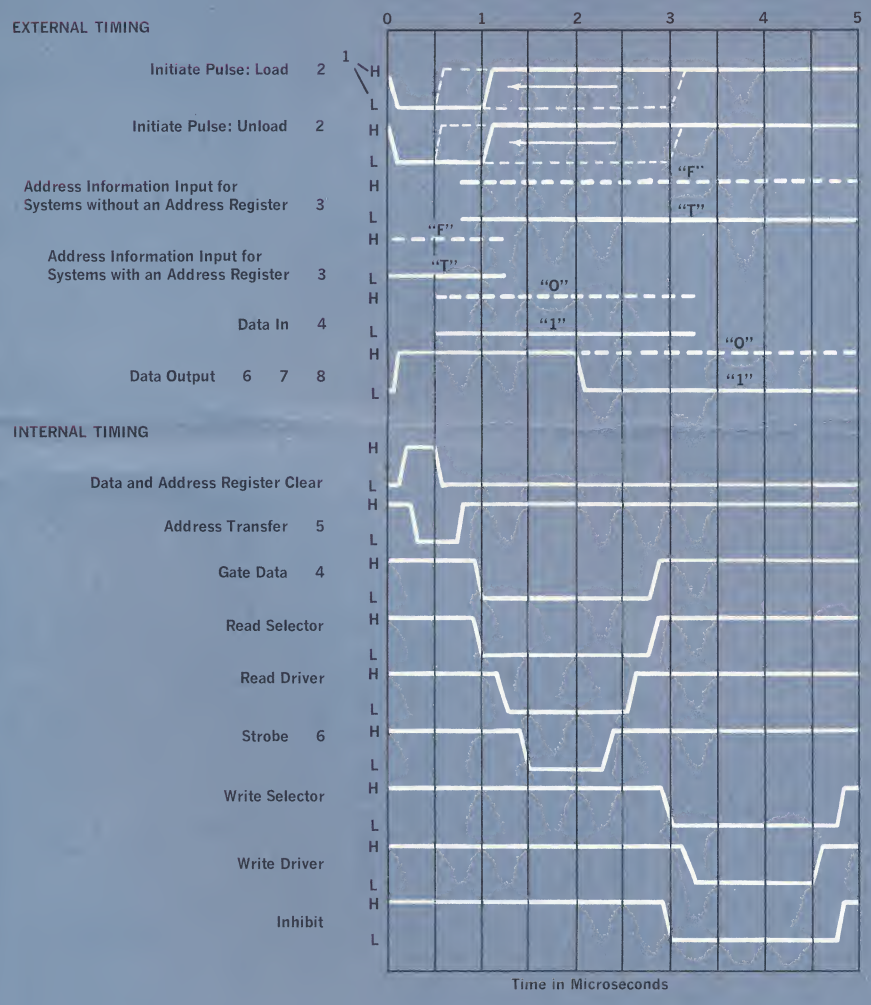
CURRENT REQUIREMENTS FOR TYPICAL SYSTEMS

SYSTEM	+3.6 Voltage ± 5%	+12 Voltage ± 2%	−12 Voltage ± 5%
128 Word Memory			
2 Bits/Word	.52 Amps (41 ma)	.62 Amps	.04 Amps (3 ma)
14 Bits/Word	.92 Amps (95 ma)	1.59 Amps	.14 Amps (6 ma)
26 Bits/Word	1.31 Amps (149 ma)	3.05 Amps	.25 Amps (10 ma)
512 Word Memory			
2 Bits/Word	.68 Amps (50 ma)	.62 Amps	.04 Amps (4 ma)
14 Bits/Word	1.07 Amps (104 ma)	1.59 Amps	.14 Amps (7 ma)
26 Bits/Word	1.47 Amps (158 ma)	3.05 Amps	.25 Amps (11 ma)
2048 Word Memory			
2 Bits/Word	.82 Amps (59 ma)	.62 Amps	.04 Amps (5 ma)
14 Bits/Word	1.22 Amps (113 ma)	1.59 Amps	.14 Amps (8 ma)
26 Bits/Word	1.61 Amps (167 ma)	3.05 Amps	.25 Amps (12 ma)

NOTE: 1. Add additional current requirements shown in parentheses when the custom interface circuits are used.

2. Add the following current requirements to the +3.6 voltage when an Address Register is used: 128 Word Memory System—140 ma, 512 Word Memory System—180 ma, 2048 Word Memory System—220 ma

TIMING CHART



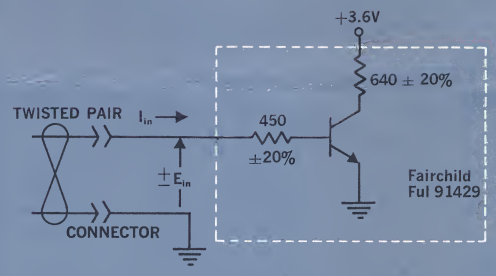
Notes

1. H = High Level +3.6V (Depends on loading).
   L = Low Level = 0 V.
2. Load and Unload Initiate Pulses enter equipment on separate lines. Both a Load and an Unload Initiate Pulse occurring during the same cycle is an illegal command. Rise time for Initiate Pulses must be 100 nsec or less at the system input. Pulse width can vary from 0.5 to 3.0 usec.
3. When the Address Register, whether internal or external, is "set," the true and false sides of the Address Register Flip-Flop are the levels indicated.
4. For Load cycle only.
5. Not applicable when system does not have an Address Register.
6. For Unload cycle only.
7. Rise time for Data Output will be 100 nsec through five feet of twisted pair.
8. Access time shown is typical; maximum access time (time when data out is stable) is 2.5 μ sec.

Standard MLA5 system interface

INPUT

This figure illustrates the "standard" input interface option. Input signals are applied directly to a Fairchild Ful 91429 integrated circuit element. Wiring to this input should be twisted pair with one wire grounded at the memory system and also grounded at the external equipment.



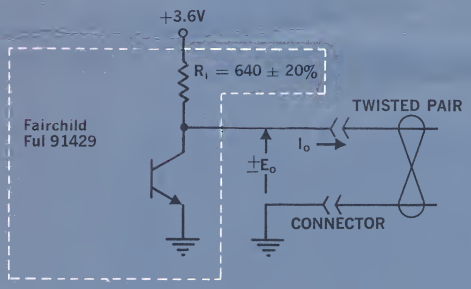
When E_{in} High: E_{in} must be greater than 1.0V but less than 4.0V

I_{in} must be greater than 0.5 ma

When E_{in} Low: E_{in} must be between −4V to +0.5V

OUTPUT

The "standard" MLA5 system output interface is shown here. Signals out are from a Fairchild Ful 91429 integrated circuit element. This "standard" output interface circuit will drive a twisted pair up to five feet in length. For longer output lines, the "custom" interface should be used. It is recommended that the MLA5 system and customer's equipment be bolted to a common grounding frame. When specifying this output interface, you must be certain that *under all conditions* the external load will accept current and never supply current!



When E_O High: I_O must not exceed 2.5 ma.
$E_O \geq 3.4 - (I_O R_l)$ volts

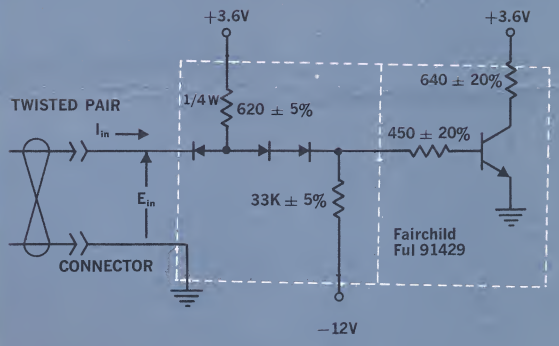
When E_O Low: Eo is less than 0.5V

NOTE: Under all conditions the external load should accept current and not supply it.

Custom MLA5 system interface

INPUT

The "custom" interface circuit will mate with most positive (above ground) and ground signal levels. This input interface must be specified if input signals do not supply current as is done using the "standard" interface. As seen in this diagram, a separate bias network supplies the Fairchild Ful 91429 integrated circuit element with the necessary drive current.

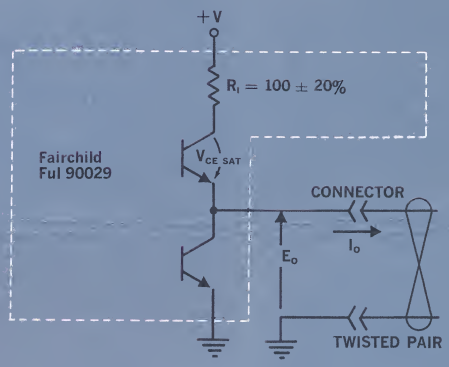


When E_{in} Low: E_{in} must be less than 1.0V
I_{in} will be less than −5.5 ma.

When E_{in} High: E_{in} must be greater than +2.5V and less than +11V.
I_{in} will be less than +100 uA.

OUTPUT

The "custom" output interface circuit is a Fairchild 90029 micrologic unit. It will drive a twisted pair up to 10 feet in length. The collector voltage (+V) illustrated on this diagram is the logic level voltage of the customer's equipment, between the limits of three and 11 volts. This arrangement assures a voltage output compatible with the remainder of the data-processing equipment. Other voltage and current limitations are called out on the diagram.



The custom interface output circuit is a Fairchild Ful 90029 micrologic unit.

+V = logic level voltage supplied by customer.

$3.0V \leq +V \leq 11V$

NOTE: WHEN $+V \geq 6V$ THE FUL 90029 MAY BE DAMAGED IF OUTPUT IS GROUNDED.

When E_O Low: E_O will be less than 0.5V.
$I_O \leq -11$ ma.

When E_O High: I_O cannot exceed 11 ma out of the interface pin.

$E_O = +V - (I_O R_l + V_{CE\ SAT})$

$V_{CE\ SAT} \leq 0.5V$

Fabri-Tek representatives are ready to solve your memory problems

Call the one nearest to you!

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For all of your requirements in non-rotating memories, look to Fabri-Tek!

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Printed in U.S.A.

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Systems Consultant
Box 1546
Poughkeepsie, N. Y. 12603

OUR REFERENCE: B1202

DATED: March 27, 1965

REFERENCE: Plug-in Integrated Memory

DEAR SIR:

Attached is the technical information you requested.

May we at be of further service to you:

- Technical assistance from one of our applications engineers on your particular application?
- Price and delivery information?

IN ORDER THAT WE DO NOT CONTACT YOU UNNECESSARILY, MAY WE SUGGEST YOUR RETURNING THE ENCLOSED REPLY CARD.

Very truly yours,

Robert F. Stahl, Jr.
General Sales Manager

YOUR NEAREST FABRI-TEK SALES OFFICE:

Wild and Associates
1519 Northern Boulevard
Roslyn Long Island New York

PLEASE REPLY TO: AMERY, WISCONSIN 54001 • Telephone 715-268-7155 • TWX 715-292-0900

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☐ CORRECT TO

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COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP CODE _____

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- ☐ We received the data you sent
- ☐ Information is adequate
- ☐ Add my name to mailing list
- ☐ We need additional information – call me
- ☐ This is for an immediate requirement
- ☐ Need price and delivery information
- ☐ Need technical assistance
- ☐ This is for a future project due Date: _____
- ☐ We need some application assistance
- ☐ This is for literature files only

T. Nelson
Systems Consultant
Box 1546
Poughkeepsie, N. Y. 12603

OUR REFERENCE B1202

DATED March 27, 1965

First Class
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Sys Cons
Box 1546
Poughkeepsie, New York

Attn: T Nelson

OUR REFERENCE: B0332

DATED: April 23, 1965

REFERENCE: Introducing

DEAR SIR:

Attached is the technical information you requested.

May we at be of further service to you:

- Technical assistance from one of our applications engineers on your particular application?
- Price and delivery information?

IN ORDER THAT WE DO NOT CONTACT YOU UNNECESSARILY, MAY WE SUGGEST YOUR RETURNING THE ENCLOSED REPLY CARD.

Very truly yours,

Robert F. Stahl, Jr.
General Sales Manager

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☐ MY NAME AND ADDRESS IS CORRECT

☐ CORRECT TO

NAME _____

DEPT. _____ PHONE NO. _____

COMPANY _____

ADDRESS _____

CITY _____ STATE _____ ZIP CODE _____

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- ☐ This is for literature files only

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Poughkeepsie, New York

Attn: T Nelson

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Coincident-current core memory stacks...

by FABRI-TEK

Fabri-Tek offers this brochure to help you to specify core memory planes for your particular requirements. The most commonly used memory plane configurations have been listed, and the most common memory core capacities are offered here. Fabri-Tek builds many other types, so if the planes described within do not meet your requirements, just ask your local Fabri-Tek representative to solve the problem.

Physical and electrical specifications are provided for individual planes. Information is also provided to permit you to order multi-plane stacks. The primary use of this book is to identify by part number the core frame configuration which matches your system's general physical and electrical needs. Then, by specifying plane configuration and quantity, you can order the exact stack design you require.

Every Fabri-Tek memory stack is manufactured to rigid quality assurance specifications. Every core and every wire is 100-percent dynamically inspected three times before shipment. Many temperature-compensated designs are available and wide-temperature cores may be had to suit special requirements. Whatever your core memory applications are, look to Fabri-Tek for the reliable, economical and prompt answer.

How to order a Series F Coincident-current Memory Plane to match your requirements

1 The first element in the part number is made up of a letter and two digits representing component type and capacity. F stands for coincident current plane and 08 indicates a capacity of 8,192 bits.

FOR CORE CAPACITY OF:	SPECIFY:
4,096 cores	F07
8,192 cores	F08
16,384 cores	F09

2 A variety of frame types are available in the F series. These are described on page 3. Select a type within the capacity range you require, then specify by letter.

3 After selecting a frame type, choose a core that matches your requirements. The table on page 4 lists eight core types. Core spacing for your frame will determine the core size which can be used. Frame type J, for example, has 50-mil spacing and can therefore be fabricated with 50-, 30- or 20-mil cores. Frame type M is a 30-mil frame and will take only 30- or 20-mil cores.

4 The F series memory plane is available in four inhibit wiring configurations. Specify type 00, 01, 10 or 11 according to the data shown on page 6.

5 Interconnection wiring between core mats is available in two ways for types F08 and F09. Select a configuration from page 6, then specify type 0 or 1 as the fifth element of your part number. If you are ordering a Series F07 plane, specify type 0.

6 The sixth element in the part number describes accessories. Specify 0 for no accessory, 1 for heater, and 2 for ground plane, according to the data on page 6.

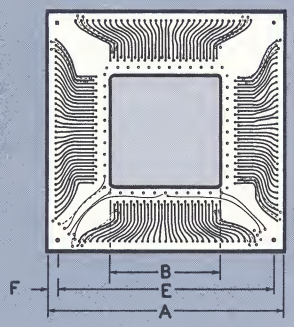
F09 M 3A 00 1 0

Typical part number describing coincident current plane with 16,384 core capacity, type M (open frame) with type A 30-mil cores, type 00 inhibit wiring, type 1 interconnecting wiring, and no heater or ground plane.

WHEN YOU HAVE SELECTED YOUR SPECIFIC PLANE TYPE, REFER TO PAGE 7 FOR MULTI-PLANE STACK ORDERING INFORMATION.

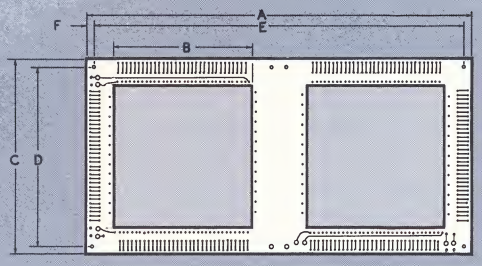
Frame Styles

OPEN OR SOLID



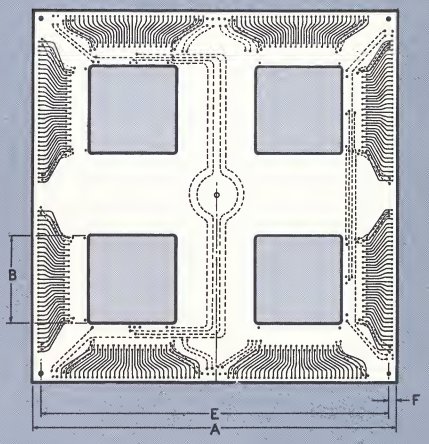
4,096-Core Capacity
Frame Styles: A,B,C,D

OPEN OR SOLID



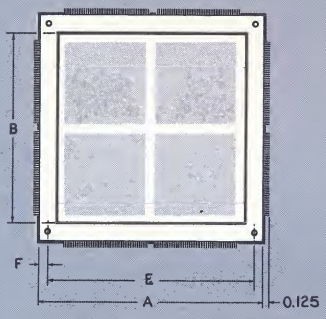
8,192-Core Capacity
Frame Styles: G,H,J,K

OPEN OR SOLID



16,384-Core Capacity
Frame Styles: L,M,N,P

EXTENDED PIN



4,096-Core Capacity
Frame Styles: E,F

16,384-Core Capacity
Frame Styles: Q,R

To Specify Frame Style and Capacity

1. Determine core capacity. As an example, should you require a 16,384-core capacity plane, you will have a range of six frames to choose from.

2. Select a suitable frame style and core spacing. An open frame, 30-mil spacing would be a typical style within the F09 series.

3. Specify the corresponding letter. In the case of the example in step 2, this would be frame M.

SELECT FRAME FROM TABLE

ORDER TYPE	FRAME STYLE	CORE SPACING (MILS)	PLANES PER INCH (STACKED)	DIMENSIONS (INCHES)						
				A	B	C	D	E	F	
A	Open	50	6	4.625	3.250	—	4.300	—	0.162	F07 SERIES (4,096-Core Capacity)
B	Open	30	6	4.000	2.000	—	3.800	—	0.150	
C	Solid	50	6	4.625	—	—	4.300	—	0.162	
D	Solid	30	6	3.960	—	—	2.800	—	0.580	
E	Extended Pin	30	8	3.075	2.325	—	2.700	—	0.187	
F	Extended Pin	20	8	2.700	1.950	—	3.236	—	0.187	
G	Open	50	6	9.300	3.425	4.625	4.300	8.975	0.162	F08 SERIES (8,192-Core Capacity)
H	Open	30	6	8.000	2.000	4.000	2.800	6.800	0.600	
J	Solid	50	6	8.372	—	4.625	4.300	8.050	0.162	
K	Solid	30	6	8.000	—	4.000	2.800	6.800	0.600	
L	Open	50	6	9.300	3.450	—	8.975	—	0.167	F09 SERIES (16,384-Core Capacity)
M	Open	30	6	8.200	2.016	—	7.850	—	0.175	
N	Solid	50	6	8.200	—	—	7.850	—	0.175	
P	Solid	30	6	8.200	—	—	7.850	—	0.175	
Q	Extended Pin	30	8	4.995	4.245	—	4.620	—	0.187	
R	Extended Pin	20	8	4.650	3.900	—	4.275	—	0.187	

Core Types

To Specify Core Type

1. Select core type in a size compatible with the frame selected on page 3.
2. Order core type, by number and letter, that fits your requirements.

	50 MIL			30 MIL			20 MIL	
SPECIFY NUMBER AND LETTER	5A	5B	5C	3A	3B	3C	2A	2B
Full write and read drive current (I_m=MA±1%)	530	450	400	640	540	475	870	640
Disturb/write current (I_d=MA±1%)	320	265	245	360	290	285	435	385
Pulse rise time (T_r=μsec±10%)	0.2	0.2	0.2	0.1	0.1	0.1	0.05	0.05
Pulse duration (T_d=μsec±10%)	2.0	2.0	2.0	0.5	0.6	.05	0.25	0.40
Undisturbed ONE response (UV_1=MV)	55 min 75 max	50 min 75 max	45 min 70 max	35 min 70 max	37 min 72 max	35 min 45 max	36 min 48 max	28 min 38 max
Disturbed ZERO response (dV_2=MV)	14 max	15 max	11 max	9 max	10 max	11 max	10 max	8 max
Switching Time T_s=μsec)	0.85 min 1.05 max	0.82 min 0.98 max	1.05 min 1.25 max	0.39 min 0.43 max	0.38 min 0.46 max	0.38 min 0.48 max	0.16 min 0.22 max	0.22 min 0.28 max
Peaking Time (T_p=μsec)	0.45 min 0.55 max	0.40 min 0.50 max	0.53 min 0.63 max	0.19 min 0.25 max	0.21 min 0.27 max	0.20 min 0.26 max	0.08 min 0.12 max	0.11 min 0.15 max
Dimensions (MILS)	50x30x15			30x20x7			23x15x5	

Test Criteria For ELR Properties

Measurements were made using the relationships shown at the right. For example, 50-mil plane measurements were made as follows:

1. Drive line. Drive a ½ I_m current pulse through a drive line. Determine inductance (L) by measuring the inductive portion of the voltage across the length of the line with the rise time equal to 0.4 μsec.

$$L=\frac{V_L\,(t_r)}{\triangle I} \qquad \text{where} \qquad \triangle I=0.8\,(½\,I_m)$$

With t_r=0.2 μsec measure the peak back voltage.

This is the value of EAC under normal operating conditions.

	50 mil	30 mil	20 mil
I_D	½ I_m	½ I_m	½ I_m
t_r (L)	0.4 μsec	0.2 μsec	0.1 μsec
t_r (EAC)	0.2 μsec	0.1 μsec	0.05 μsec
I_{Inh}	½ (.9 I_m)	½ (.9 I_m)	½ (.9 I_m)
t_r (L)	0.6 μsec	0.3 μsec	0.15 μsec
t_r (EAC)	0.3 μsec	0.15 μsec	0.075 μsec

2. Inhibit lines are same as for drive lines except current pulse is ½ (0.9 I_m),

t_r (L)=0.6 μsec, and t_r (EAC)=0.4 μsec.

Revision Note

Please note the following changes:

Page 3: Select Frame Table is incorrect. Should be:

SELECT FRAME FROM TABLE

ORDER TYPE	FRAME STYLE	CORE SPACING (MILS)	PLANES PER INCH (STACKED)	DIMENSIONS (INCHES)						
				A	B	C	D	E	F	
A	Open	50	6	4.625	3.250	—	—	4.300	0.162	F07 SERIES (4,096-Core Capacity)
B	Open	30	6	4.100	2.000	—	—	3.800	0.150	
C	Solid	50	6	4.625	—	—	—	4.300	0.162	
D	Solid	30	6	3.960	—	—	—	2.800	0.580	
E	Extended Pin	30	8	3.075	2.325	—	—	2.700	0.187	
F	Extended Pin	20	8	2.700	1.950	—	—	2.325	0.187	
G	Open	50	6	9.300	3.425	4.625	4.300	8.975	0.162	F08 SERIES (8,192-Core Capacity)
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P	Solid	30	6	8.200	—	—	—	7.850	0.175	
Q	Extended Pin	30	8	4.995	4.245	—	—	4.620	0.187	
R	Extended Pin	20	8	4.650	3.900	—	—	4.275	0.187	

New address: Fabri-Tek Incorporated

5901 South County Road Eighteen

Minneapolis, Minnesota 55436

Telephone: 612-935-8811

TWX: 910-576-2913

Bulletin 6533

July 6, 1966

FABRI-TEK INCORPORATED • 5901 SOUTH COUNTY ROAD 18 • MINNEAPOLIS, MINNESOTA 55436 • TEL. 612-935-8811

November 30, 1966

Mr. T. Nelson
Systems Consultant
Box 1546
Poughkeepsie, New York 12603

Dear Mr. Nelson:

Enclosed is the stacks "Cook Book" you requested.

Thank you for your interest in FABRI-TEK.

If we can be of further assistance, please let us know.

Sincerely,

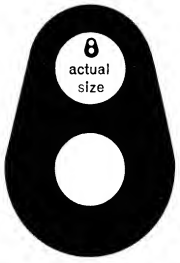
Roger Harmon

Roger Harmon
Advertising Manager

RH:sm

Enc.

SHMOO TRANSFLUXOR CORES FOR NON-DESTRUCT COINCIDENT CURRENT MEMORIES.

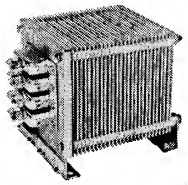


At last; a two-aperture, coincident current ferrite core for NDRO memories — the Shmoo. Developed by Electronic Memories, the Shmoo transfluxor opens new design areas to memory systems engineers. For instance, you can use the same coincident current drive circuitry for a combination non-destructive Shmoo core/scratch pad toroid core memory. With the Shmoo, you get a read hole that has physical and electrical characteristics that match a 50-mil toroid. And, because the Shmoo is shmoo-shaped and bottom heavy, it can be easily oriented for automatic testing and stringing.

The Shmoo core is available off the shelf, or in special arrays, stacks and completely assembled memories.

A STACK BUYER'S GUIDE

to getting fast delivery of 30 or 50-mil coincident current memory stacks and controlling cost and frustration levels.



Electronic Memories is now delivering standard, off-the-shelf memory stacks in a versatile choice of word and bit configurations. Ordering one of these standard stacks is as easy as this:

1. Choose a core from the chart below.

		30 mil Cores			50 mil Cores			
TYPE		31-100	31-103	31-108	51-101	51-110	51-119	51-113
RECOMMENDED DRIVE CURRENTS @ 25°C	DRIVE (ma turns)	500/250	580/290	720/360	520/260	500/250	400/200	380/190
	CYCLE TIME**	1.5-3	1.5-3	1.5-3	3-4	5-6	6-8	6-8
	RISE TIME*	0.05	0.10	0.10	0.15	0.20	0.50	0.20
	PULSE TIME*	0.6	0.6	0.6	1.0	2.0	3.0	2.0
TYPICAL OUTPUT SIGNALS	uV_1 (mv)	60	58	62	110	68	90	54
	dVz (mv)	8	6	5	15	8	5	8
	PEAK TIME*	0.17	0.24	0.21	0.32	0.52	0.75	0.65
	SWITCH TIME*	0.37	0.38	0.39	0.65	1.02	1.25	1.35

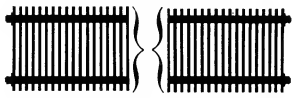
*Microseconds **Memory systems

2. Select a word size.

☐ 256 ☐ 512 ☐ 1024 ☐ 2048 ☐ 4096

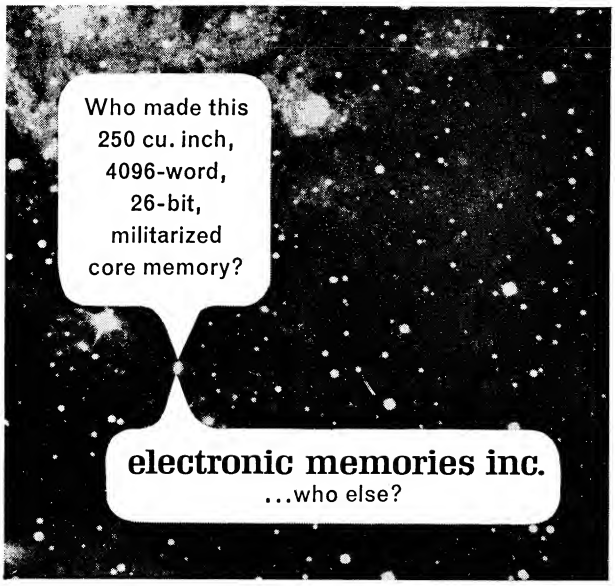
Typical Dimensions (4096 words)
30-mil array, 3.25" x 3.25"
50-mil array, 4.625" x 4.625"

3. Specify # of arrays in stack.

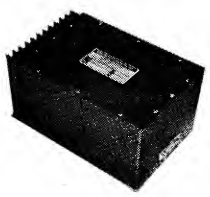


Typical Dimensions (4096 words x 24-bits)
30-mil stack, 3.62" x 4.4" x 4.3"
50-mil stack, 4.8" x 5.45" x 6.95"

4. Request off the shelf delivery for standard arrays and stacks. Special applications are shipped in a matter of weeks.



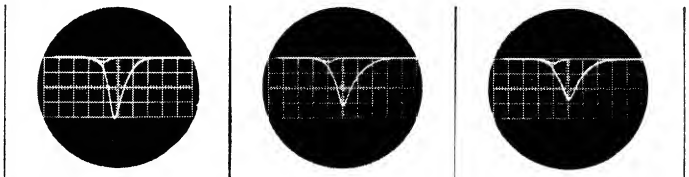
Electronic Memories' standardized core memories give economical random access militarized operation over a −55°C to +100°C range. These memories are available in two high density packaging versions: The pluggable version has modular, welded plug-in circuits for simplified maintenance in ground based and aerospace applications such as support and control systems for tactical weaponry. The other version has all sub-assemblies incorporated in welded modules for maximum package density and reliability. Both versions utilize standard components in special high density circuit designs to achieve maximum miniaturization without sacrifice of field proven reliability. These memories use Isodrive* cores to achieve dependable operation over a wide temperature range.



*Registered

NEW LOCATION *12621 Chadron Avenue, Hawthorne, California*

WIDE TEMPERATURE RANGE CORES



+100°C
Actual test oscillogram with 50-mil core in boiling water

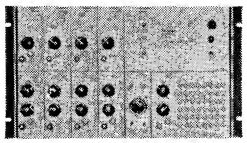
+25°C
Scale for oscillograms: 50 mv/cm, .25 usec/cm; rise time: .2 usec.

−55°C
Actual test oscillogram, with 50-mil core in dry ice and alcohol

Electronic Memories' Isodrive* cores provide excellent signal/noise ratios and operating margins over temperature ranges from −55°C to +100°C with constant drive currents. Available in both 30-mil and 50-mil types, they feature fast switching, high output, low noise and high disturb ratio which exceeds 0.60 from −70°C to +100°C at constant drive current.

*Registered

Test magnetics quicker, easier, cheaper . . .



Who says it takes a large expensive tester to design and/or test magnetic cores and circuits? Electronic Memories' 100-Series testers weigh about 35 pounds, cost as little as $4,500, and do everything the big expensive testers can do, and then some. These testers provide up to 1200 ma current pulses with rise times as fast as 50 nanoseconds over a wide range of programs. If you haven't seen our technical bulletin on the 100-Series testers, may we send you a copy?

FABRI-TEK Representatives are ready to help you solve your memory problems . . .

Call the one nearest you!

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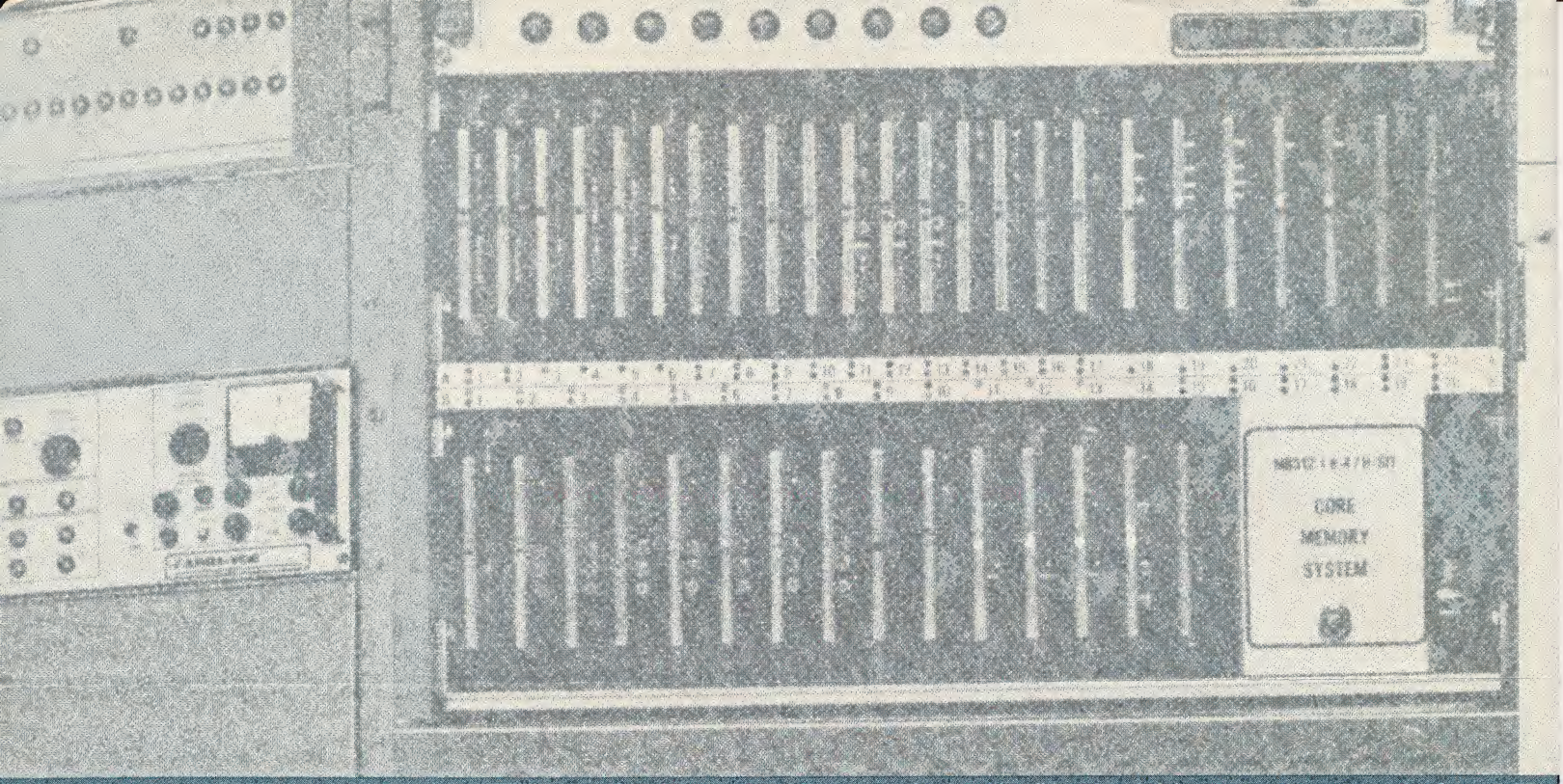

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Fabri-Tek has the core memory system you need, no matter what your requirements are.

BIG Are you looking for mass memories?—We can give you up to 20 million bits with our Series MT System.

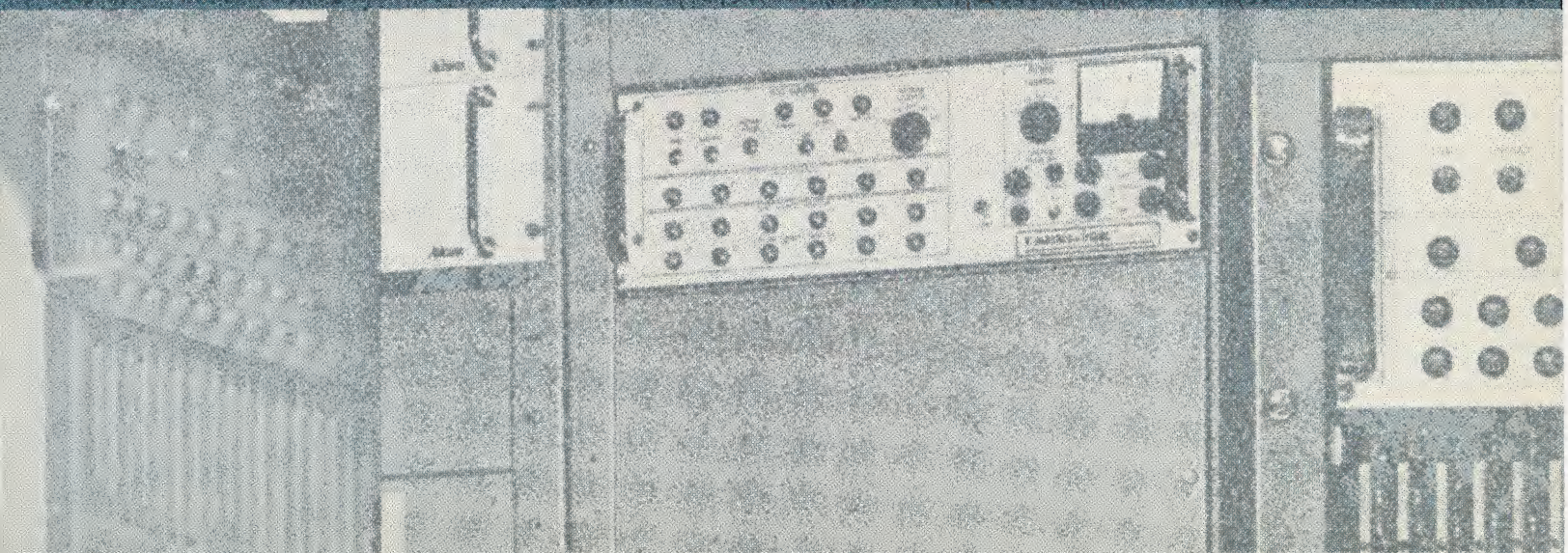
SMALL If you're looking for an inexpensive, small memory to provide the "heart" of small systems, ask for the ML Series Integrated Memory System.

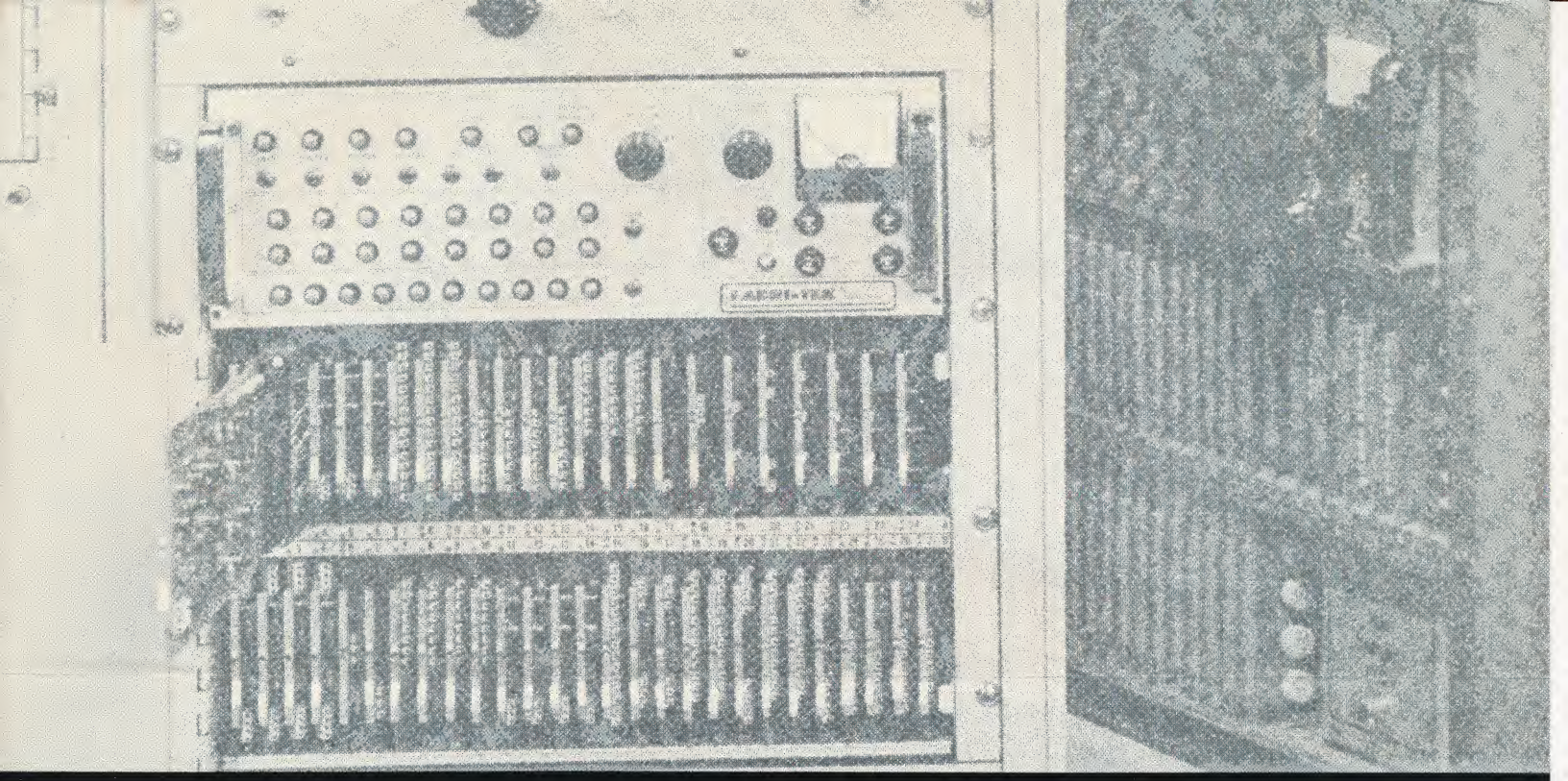
SLOW Want coincident-current memory systems in the 5-microsecond range or slower? Our Series MA and MS (all silicon) are your answer.

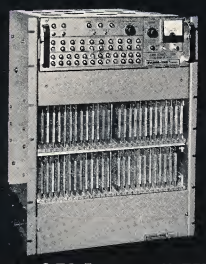
FAST Need 2-microsecond speeds or faster? The Fabri-Tek MF Series is a 1-microsecond system with coincident current organization and exceptionally wide operational margins. For very fast 300-nanosecond cycles, we have the FFM-202 Thin-film memory systems.

There are many more! Fabri-Tek has a magnetic, non-rotating memory system to match any set of requirements you can name. Customer's colors, nameplates, and panel layout are matched to provide a unified appearance when the Fabri-Tek system is installed. We'll use special parts which you specify—even use parts you may wish to supply.

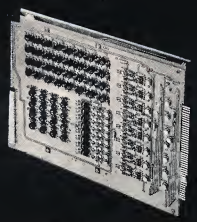
If you have a requirement for a memory system, look to Fabri-Tek for the quick, reliable, and economical answer. Write, call, or wire Fabri-Tek Incorporated, Amery, Wisconsin. COngress 8-7155 (Area 715). TWX: 715-292-0900.



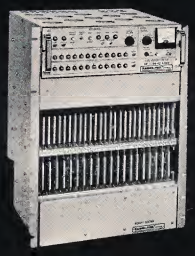




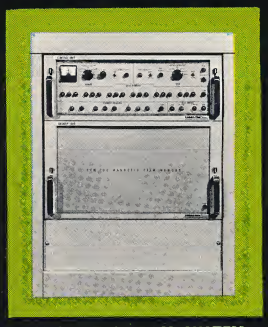
SERIES MA 2 TO 5 USEC SYSTEM IS A "STANDARD" IN THE COMPUTER INDUSTRY



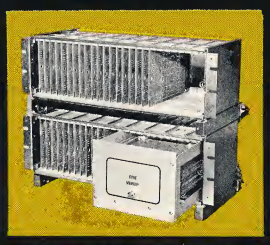
SERIES ML INTEGRATED, PLUG-IN MEMORY SYSTEM FOR FAIRCHILD



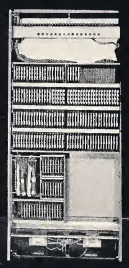
NEW MF SYSTEM HAS 1-USEC CYCLE TIME AND ALL SILICON SEMI-CONDUCTORS



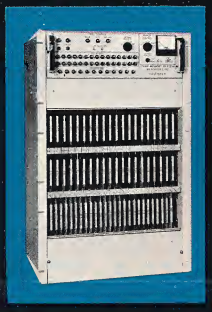
FFM-202 THIN-FILM SYSTEM— THE FIRST PRODUCTION THIN-FILM MEMORY



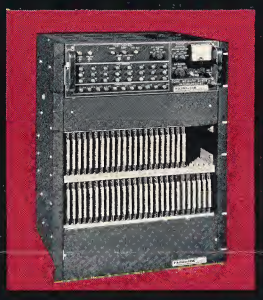
FABRI-TEK SUPPLIES MANY CUSTOMERS WITH THIS "HEART" OF A MEMORY SYSTEM —STACK AND DRIVE CIRCUITS



A 2-MICROSECOND, 8192 x 50-BIT SYSTEM FOR G.E.

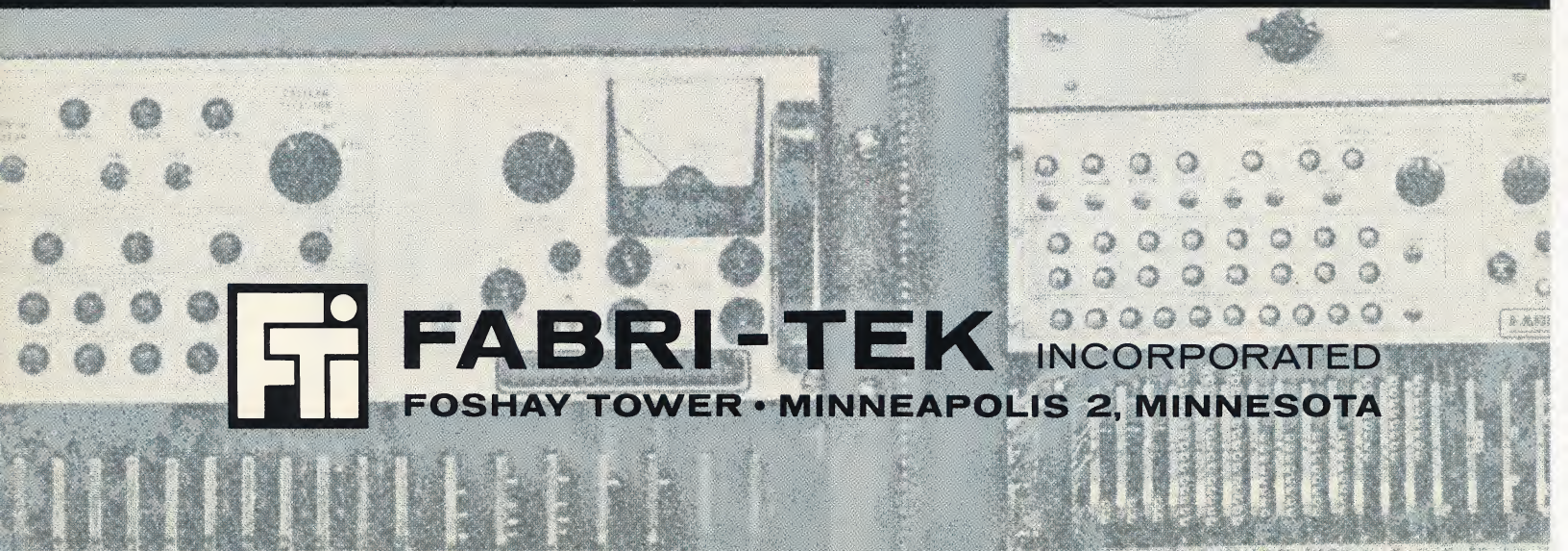


A 4096 x 30-BIT SYSTEM FOR THE ADAGE AMBILOG 200



A 2048 x 24-BIT SYSTEM FOR BECKMAN —PAINTED WITH BECKMAN "BLACK" TO MATCH A SYSTEM

50,000-BIT THIN-FILM MEMORY SYSTEM FOR THE U. S. NAVY



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